REMARKS

This application has been reviewed in light of the Office Action dated September 17, 2008.

Claims 1-12 , 21 and 22 are presented for examination. Claims 13-20, which were previously withdrawn from consideration by the Examiner, have been cancelled without prejudice to their being presented in a divisional application. Claim 1, which is the only remaining independent claim, has been amended. Favorable review is respectfully requested.

Independent claim 1 has been amended to explicitly recite a package including a lead frame including an electrically conductive substrate; the lead frame has planar first and second sides. An array of lands protrude from the first side surface; an array of chip attach sites protrude from the second side surface. Furthermore, the lands and chip attach sites are integral with the substrate in a monolithic electrically conductive structure. In addition, the array of lands has a larger lateral extent than the array of chip attach sites. Support for this amended claim language appears in the specification at least at page 7, lines 1-4 and 8-11; page 7, line 30, to page 8, line 3; and FIGS. 4, 5A, 5B and 7.

In discussing the language of claim 1 (Office Action, page 3), the Examiner suggested that "formed from" introduced a process limitation which did not carry patentable weight. While the applicants do not agree with this statement, this phrase has been removed from claim 1. Claim 1, as amended, positively recites a lead frame including a substrate, and where lands and chip attach sites protrude from first and second side surfaces of the lead frame.

Claims 1-5, 9-12 and 21 were rejected under 35 U.S.C. § 103(a) as unpatentable over Choi (U.S. Pat. Application Publication No. 2002/0105077) in view of Kuo et al. (U.S. Pat. Application Publication No. 2002/0197842). The applicants respectfully submit that amended independent claim 1 is patentably distinct from the cited art, for the following reasons.

The Examiner points to FIG. 1 in Choi as disclosing a lead frame with a substrate, lands and routing circuits as claimed in claim 1. This statement is respectfully traversed. FIG. 1 of Choi, which the Choi reference itself treats as prior art, clearly does not disclose or suggest the package of the present invention. The substrate (10) shown in this figure is a plastic resin, which clearly is not electrically conductive. This substrate has copper printed circuit patterns (14) formed on the top and bottom surfaces thereof (Choi, paragraph 0008). Furthermore, the

top surface of this substrate (which has wirebond sites for connecting to a chip) clearly does not have chip attach sites protruding from a surface, as required by claim 1. To the contrary, FIG. 1 of Choi appears to have wirebonding attachment sites planar with the pattern 14. On the other side of the substrate shown in FIG. 1 of Choi, solder balls 13 are connected to the printed circuit pattern. No part of the copper printed circuit pattern protrudes from the side of the substrate. Even if the solder balls 13 could be viewed as lands protruding from the surface, the solder balls and the substrate clearly do not form a monolithic electrically conductive structure.

The package claimed in claim 1 recites a lead frame, substrate, and connection to a semiconductor device consistent with a "flip chip" approach, the details of which are discussed in the specification. In contrast, FIG. 1 of Choi et al. is understood to disclose a conventional semiconductor package using wirebond sites, as opposed to a flip chip arrangement with an array of chip attach sites. This conventional arrangement clearly is concerned with a different packaging scheme from the present invention. The Examiner appears to be in agreement on this point, stating that Choi does not teach chip attach sites directly electrically interconnected to input/output pads on a semiconductor device. The reason for this is clear to those skilled in the art; Choi is concerned with a wirebond type package, whereas claim 1 is directed to a package consistent with a flip-chip approach. This is immediately evident from a comparison of Choi FIG. 1 with FIG. 7 of the specification. In Choi FIG. 1, wirebonds connect to sites on the device 6 on top of the device (the side facing away from the lead frame). In FIG. 7 of the specification, direct connections are made to sites on the device 28 on the underside of the device (the side facing toward the lead frame).

The conventional, wirebond package shown in FIG. 1 of Choi does not disclose or suggest (1) a conductive substrate; (2) chip attach sites opposite input/output pads of a device; (3) lands and chip attach sites protruding from planar surfaces; (4) lands and chip attach sites integral with the substrate; or (5) a monolithic electrically conductive structure including the substrate, lands and chip attach sites. Accordingly, the package of claim 1 is not rendered obvious by the conventional package discussed in Choi.

Kuo et al. is understood to disclose a method for forming solder bumps. Kuo et al. does not disclose or suggest a conductive substrate for a package, and in particular does not suggest a monolithic lead frame structure as recited in claim 1. Clearly, one using the process of Kuo et al. would arrive at a conductive structure with solder bumps attached to it, as opposed to a

monolithic structure. Kuo et al. therefore does not remedy the defects of Choi as a reference against amended claim 1. It therefore is submitted that independent claim 1 is not rendered obvious by the cited references, considered either singly or in combination.

Dependent claims 6, 7 and 22 were rejected as obvious from the combination of Choi and Kuo et al. with Shimanuki et al (U.S. Pat. Application Publication No. 2002/0168796); dependent claim 8 was rejected as obvious from the combination of Choi and Kuo et al. with Sakamoto et al. (U.S. Pat. No. 6,967,401). Neither of these additional references suggests a monolithic lead frame, or an arrangement of lands and chip attach sites where the array of lands has a larger lateral extent than the array of chip attach sites. In addition, neither Shimanuki et al. nor Sakamoto et al. is concerned with a flip-chip arrangement; in particular, neither of these references suggests an array of chip attach sites opposite the input/output pads of a device. Accordingly, neither of these references, even when considered in combination with Choi and Kuo, renders obvious the package of independent claim 1.

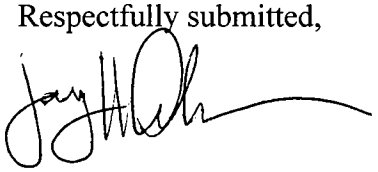
The other claims in the application are dependent from the independent claim discussed above and are believed to be patentable for the same reasons. Since each dependent claim is directed to a separate aspect of the invention, however, the individual consideration of each claim on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, favorable consideration and early passage to issue of the application are respectfully requested.

This Amendment is being submitted on the first business day following the expiration of two months from the date of the final Office Action. Accordingly, the period for reply will expire at three months from the date of the Office Action or on the date an Advisory Action is mailed, whichever is later. MPEP § 706.07(f).

The applicants' undersigned attorney may be reached by telephone at 212-551-2625. All correspondence should continue to be directed to the address given below, which is the address associated with Customer Number 27267.

Respectfully submitted,



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